



10th International Workshop on *Software & Compilers for Embedded Systems*

April 20, 2007
Palais des Congrès Acropolis,
Nice, France

Heiko Falk, Peter Marwedel

Co-located with  **DATE**⁰⁷



About SCOPES 2007

- 30 Submissions in total
- from 14 countries
- in 4 continents (Australia, Europe, N. America, S. America)
- 12 Submissions accepted
- *Acceptance Rate: 40%*
- Held as DATE Friday Workshop

- Sponsored by:



- In cooperation with:





Session 1: Stream- and data-flow based computing

Session Chair: Jörg Henkel

- Efficient Buffer Capacity and Scheduler Setting Computation for Soft Real-Time Stream Processing Applications
M. Bekooij, M. Wiggers, J. v. Meerbergen
- Modelling Run-Time Arbitration by Latency-Rate Servers in Dataflow Graphs
M. Wiggers, M. Bekooij, G. Smit
- Automatic partitioning and mapping of stream-based applications onto the Intel IXP Network Processor
S. Meijer, B. Kienhuis, J. Walters, D. Snuijf



Session 2: Memory-aware compilation

Session Chair: Marco Bekooij

- Optimization of Dynamic Data Structures in Multimedia Embedded Systems Using Evolutionary Computation
D. Atienza, C. Baloukas, L. Papadopoulos, C. Poucet, S. Mamagkakis, J. I. Hidalgo, F. Catthoor, D. Soudris, J. Lanchares
- Operating system integrated energy aware scratchpad allocation strategies for multiprocess applications
R. Pyka, C. Faßbach, M. Verma, H. Falk, P. Marwedel
- Systematic Intermediate Sequence Removal for Reduced Memory Accesses
C. Poucet, S. Mamagkakis, D. Atienza, F. Catthoor



Session 3: Multiprocessors and link-time optimization

Session Chair: Hans van Someren

- Whole-Program Linear-Constant Analysis with Applications to Link-Time Optimization
L. v. Put, D. Chanet, K. d. Bosschere
- Efficient Event-driven Simulation of Parallel Processor Architectures
A. Kupriyanov, D. Kissler, F. Hannig, J. Teich
- Reducing fine-grain communication overhead in multithread code generation for heterogeneous MPSoC
*L. Brisolara, S. Han, X. Guerin, L. Carro, R. Reis, S. Chae
A. Jerraya*



Session 4: Recent advances in static single-assignment representations

Session Chair: Paolo Ienne

- Optimal Chain Rule Placement for Instruction Selection Based on SSA Graphs
S. Schäfer, B. Scholz
- Interference Graphs for Procedures in Static Single Information Form are Interval Graphs
P. Brisk, M. Sarrafzadeh
- Improvements to the Psi-SSA Representation
F. d. Ferrière