Monday June 12th, 2017

12.00 – 13.15 Lunch

13.15 – 13.30 Opening
   Henk Corporaal

13.30 – 14.30 Keynote 1: Dynamically adaptive cross-layer fault-tolerant system design
   Akash Kumar

14.30 – 15.00 Coffee Break

15.00 – 16.00 Session 1
15.00  TETRiS: a Multi-Application Run-Time System for Predictable Execution of Static Mappings (full paper)
   Andrés Goens, Robert Khasanov, Marcus Hähnle, Till Smejkal, Hermann Härtig and Jeronimo Castrillon
15.30  Robust Mapping of Process Networks to Many-Core Systems using Bio-Inspired Design Centering (full paper)
   Gerald Hempel, Andrés Goens, Josefine Asmus, Jeronimo Castrillion and Ivo F. Sbalzarini

16.00 – 16.30 Coffee Break

16.30 – 18.00 Session 2
16.30  Self-Adaptive FPGA-Based Image Processing Filters Using Approximate Arithmetics
   Jutta Pirkl, Andreas Becher, Jorge Echavarria, Jürgen Teich and Stefan Wildermann
17.00  Automatic Conversion of Simulink Models to SysteMoC Actor Networks
   Martin Letras, Joachim Falk, Stefan Wildermann and Jürgen Teich
17.30  Exploiting Predictability in Dynamic Network Communication for Power-Efficient Data Transmission in LTE Radio Systems
   Peter Brand, Jonathan Ah Sue, Johannes Brendel, Joachim Falk, Ralph Hasholzner, Jürgen Teich and Stefan Wildermann
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Tuesday June 13th, 2017

8.30 – 10.30 Session 3

8.30  Automatic Tuning with Ordinal Regression  
      Biagio Cosenza, Juan Durillo, Stefano Ermon and Ben Juurlink

9.00  Numerical Accuracy Improvment by Interprocedural Program Transformation (full paper)  
      Nasrine Damouche, Matthieu Martel and Alexandre Chapoutot

9.30  Constructing HPSSA over SSA (full paper)  
      Smriti Jaiswal, Praveen Hegde and Subhajit Roy

10.00 Software Prefetching for Indirect Memory Accesses  
      Sam Ainsworth, Timothy Jones

10.30 – 11.00 Coffee Break

11.00 – 12.00 Session 4

11.00 Hybrid Latency Minimization Approach using Model Checking and Dataflow Analysis (full paper)  
      Guus Kuiper, Marco Bekooij and Philip Kurtin

11.30 Efficient FPGA Design for ICP Using the Functional Approach of CλaSH  
      Hendrik Folmer, Robin Appel, Arjan Boeijink, Rinse Wester, Jan Kuper, and Jan Broenink

12.00 – 13.00 Lunch

13.00 – 14.00 Session 5

13.00 Data Dependent Energy Modeling for Worst Case Energy Consumption Analysis (full paper)  
      James Pallister, Steve Kerrison, Jeremy Morse and Kerstin Eder

13.30 On the accuracy of near-optimal GPU-based path planning for UAVs  
      Daniele Palossi, Andrea Marongiu and Luca Benini

14.00 – 15.00 Session 6

14.00 Combining dataflow applications and real-time task sets on multi-core platforms  
      Hazem Ismail Ali, Benny Akesson and Luis Miguel Pinho

14.30 Application Mapping and Scheduling through ASPmT with Partial Assignment Evaluation  
      Kai Neubauer, Christian Haubelt, Philipp Wanko and Torsten Schaub

15.00 – 15.30 Coffee break
15.30 – 16.30 Session 7
15.30  Enabling zero-copy OpenMP offloading on the PULP many-core accelerator
        Alessandro Capotondi and Andrea Marongiu
16.00  The LPGPU2 Project - Low-Power Parallel Computing on GPUs
        Ben Juurlink, Martyn Bliss, Georgios Keramides and Jan Lucas

16.30 – 17.00 Best presentation award ceremony / Closing remarks